# Low Delay Encoding Requirement for H264/H264 Encoder

## Sub-frame Synchronization

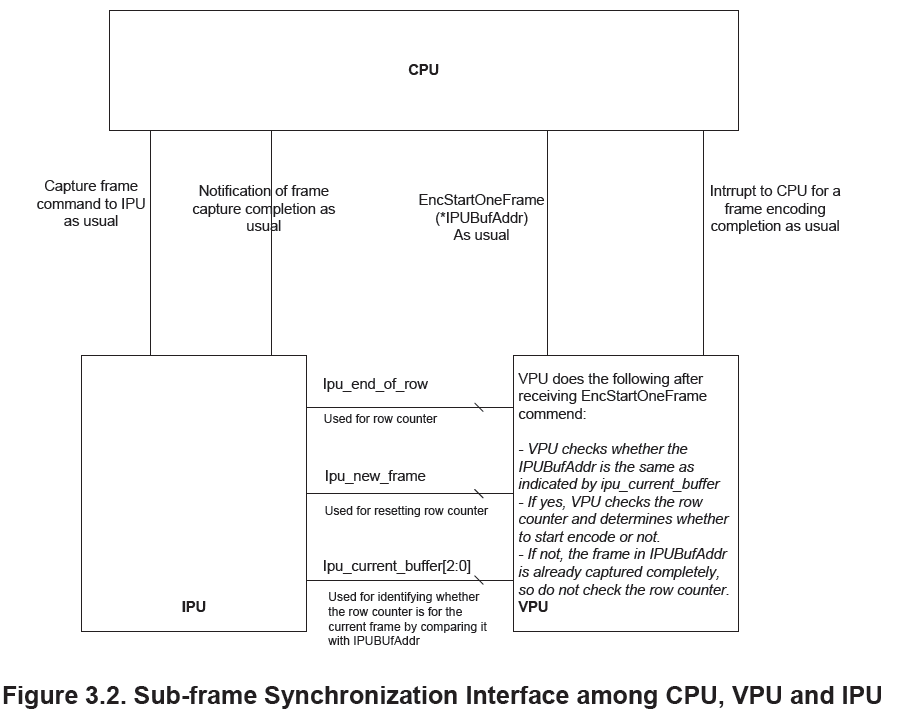
Low delay encoding contains wire-based sub-frame synchronization and reg-base sub-frame synchronization two working modes .The later chapters will mainly discuss wire-base sub-frame synchronization mode.

VPU supports sub-frame synchronization for low latency encoding by receiving dedicated sub-frame-ready signals from IPU (Image Process Unit, such as ISP) so that VPU (H264/HEVC) encoder can start encoding process as early as the minimum set of raw video data is ready.

### 1.1 wire based sub-frame synchronization

sub-frame synchronization makes VPU start encoding after a line of CTU (64 lines for HEVC) row buffer or a line of macroblock(MB for H264) row buffer is filled up by IPU, and if there are multiple raw image buffers, IPU can write raw image to one buffer while VPU is encoding with other buffer, so that the latency time caused by image buffering can be significantly reduced.

The interactions among VPU (Encoder), CPU, and IPU(ISP) is shown as follow figure.



### 1.2 IPU (ISP) to VPU Signals

There interface signals are needs between IPU and VPU, They are

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Name | From | To | Clock domain | Bit width |
| ipu\_new\_frame | IPU(ISP) | VPU(Encoder) | ISP Clock Domain | 1bit |
| ipu\_end\_of\_row | IPU(ISP) | VPU(Encoder) | ISP Clock Domain | 1bit |
| ipu\_current\_buffer[2:0] | IPU(ISP) | VPU(Encoder) | ISP Clock Domain | 3bit |

**ipu\_end\_of\_row**

An ipu\_end\_of\_row signal, which is flipped every time when the IPU completes writing a row (i.e. receives a completion acknowledgement from the DDR).

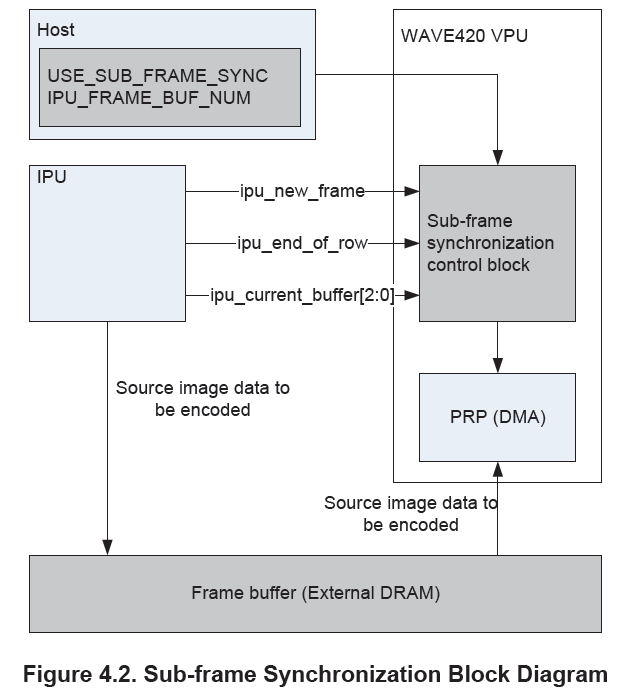
**ipu\_new\_frame**

An ipu\_new\_frame signal, which is flipped every time the IPU starts writing a new frame.

**ipu\_current\_buffer[2:0]**

An ipu\_current\_buffer[2:0] signal, indicating which buffer is currently active so that the VPU can correctly use the ipu\_end\_of\_row signal for row counter. This is a 3-line signal with each representing a current frame buffer that IPU captures frame into. Therefore, at any time, only one line is active (active high, level indication). So, the possible values for this signal should be 000 (for low active frame buffer), 001 (bit 1 high for buffer 1), 010 (bit2 high for buffer 2 active), and 100 (bit 3 high for buffer 3 active).

The interface between IPU (ISP) and VPU(Encoder) is shown in below Figure.



### 1.3 Register Control

There are three register for initializing Sub-frame Sync function.

•USE\_SUB\_FRAME\_SYNC: decide whether to use sub frame sync.

– 0: disable sub-frame synchronization.

– 1: enable sub-frame synchronization.

• REG\_SUB\_FRAME\_SYNC :

decide either register based enabling or wire based enabling.

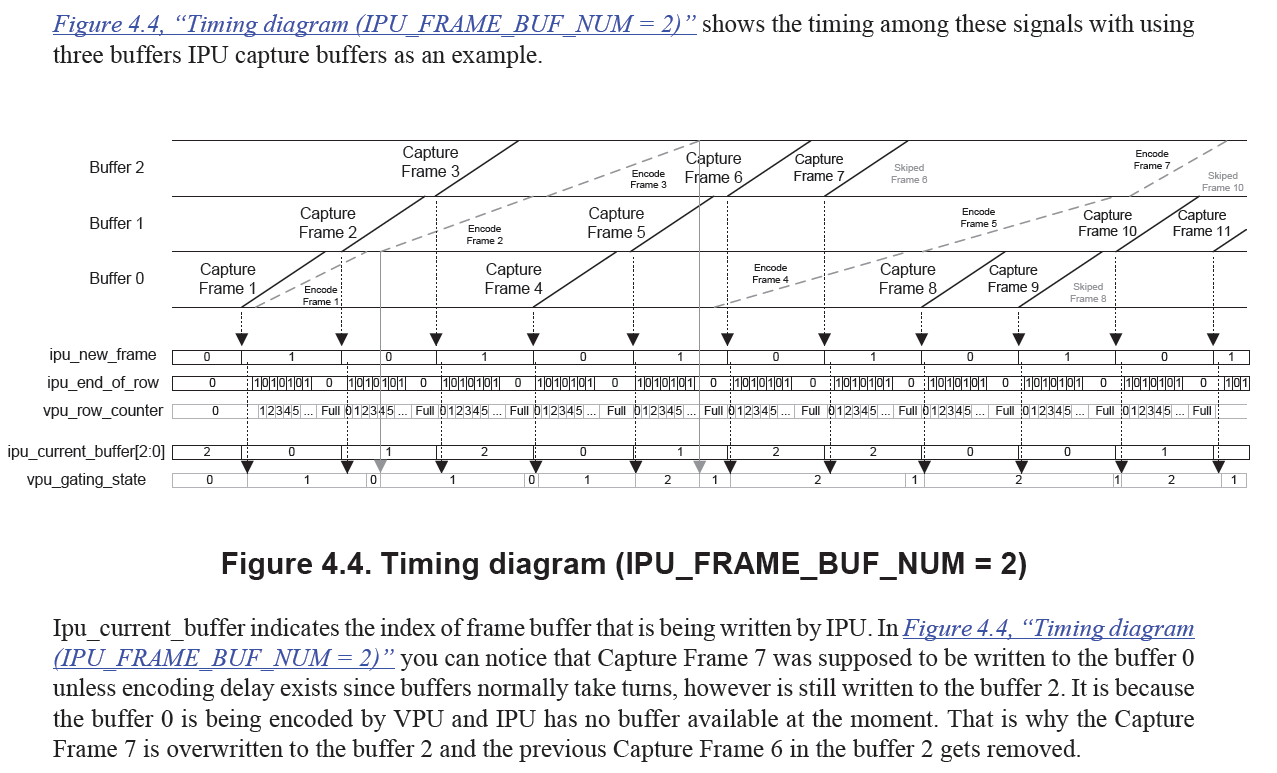
• IPU\_FRAME\_BUF\_NUM : numbe of raw image buffer

– Up to three buffers available

– Raw image buffer number = IPU\_FRAME\_BUF\_NUM + 1

### 1.4 VPU\_gating\_State

### 1.5 Timing Diagram



### 1.6 Appendix

The detail description of wire-based sub-frame synchronization mode for low delay encoding, please refer to chapter 4 of cnm-wave420-datasheet-Artosyn\_v1.12.0.pdf (HEVC) or chapter 3.1.1 of cnm-coda988-datasheet-Artosyn\_v4.10.0.pdf (H264) .

The pdf file directory are

H264: LnxShare\Video\_Share\IPs\chips\_media\CODA988\cnm-coda988-pkg-v3.7.26\02\_Hardware\Documents

HEVC: LnxShare\Video\_Share\IPs\chips\_media\WAVE420\cnm-wave420-pkg-v1.5.3\02\_Hardware\Documents